

1. A method of forming a split-gate flash memory having a non-smiling trench isolation comprising the steps of:

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providing a semiconductor substrate;

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forming a gate oxide layer over said substrate;

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forming a first polysilicon layer over said gate oxide layer;

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forming a pad oxide layer over said first polysilicon layer;

forming a first nitride layer over said pad oxide layer;

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forming and patterning a first photoresist layer over said first nitride layer to define active regions in said substrate;

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forming a trench in said substrate by etching through patterns in said first photoresist layer;

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removing said first photoresist layer;

- 24 forming a first conformal lining on the inside walls of said trench;
- 27 forming a second conformal lining over said first conformal lining on the inside walls of said trench;
- 30 depositing isolation oxide inside said trench to form shallow trench isolation (STI);
- 33 performing chemical-mechanical polishing of said substrate;
- 36 removing said first nitride layer;
- 39 removing said pad oxide layer;
- 42 forming second nitride layer over said substrate;
- 45 forming and patterning a second photoresist layer over said second nitride layer to define floating gate;
- 48 etching through patterns in said second photoresist layer to form openings in said second nitride layer exposing portions of said first polysilicon layer;

48 removing said second photoresist layer;

performing thermal oxidation of exposed said portions of
51 said first polysilicon layer through said openings in said
second nitride layer to form polyoxide hard mask;

54 removing said second nitride layer;

etching said first polysilicon layer using said polyoxide as
57 a hard mask;

forming intergate oxide layer;

60 forming a second polysilicon layer over said intergate oxide
layer;

63 forming and patterning a third photoresist layer over said
second intergate oxide layer to define control gate; and

66 etching through said patterning in third photoresist layer to
complete the forming of said split-gate flash memory.

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2. The method of claim 1, wherein said semiconductor
substrate is silicon.

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3. The method of claim 1, wherein said forming a gate oxide layer is accomplished by thermal growth at a temperature between about 800 to 1100 °C.

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4. The method of claim 1, wherein said first gate oxide layer has a thickness between about 70 to 110 angstroms (Å).

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5. The method of claim 1, wherein said forming a first polysilicon layer is accomplished with silicon source SiH_4 using LPCVD at a temperature between about 500 to 650 °C.

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6. The method of claim 1, wherein said first polysilicon layer has a thickness between about 800 to 1500 angstroms (Å).

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7. The method of claim 1, wherein said pad oxide layer has a thickness between about 100 to 250 Å.

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8. The method of claim 1, wherein said depositing a first nitride layer over said pad oxide layer is accomplished by CVD at a temperature between about 720 to 820°C by reacting dichlorosilane (SiCl_2H_2) with ammonia (NH_3).

9. The method of claim 1, wherein the thickness of said first nitride layer is between about 1200 to 2000 Å.

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10. The method of claim 1, wherein said first photoresist layer has a thickness between about 0.5 to 1.0 micrometers (μm).

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11. The method of claim 1, wherein said forming a trench in said substrate by etching through patterns in said first photoresist layer into underlying said first nitride layer, pad oxide layer, first polysilicon layer and gate oxide layer is accomplished with etch recipe comprising gases Ar, CHF₃, C₄F₈.

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12. The method of claim 1, wherein said removing said first photoresist layer is accomplished by oxygen plasma ashing.

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13. The method of claim 1, wherein said first conformal lining comprises oxide having a thickness between about 200 to 550 Å.

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14. The method of claim 1, wherein said second conformal lining comprises nitride having a thickness between about 100 to 300 Å.

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15. The method of claim 1, wherein said isolation oxide has a thickness between about 4000 to 6000 Å.

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16. The method of claim 1, wherein said removing said first nitride layer and pad oxide layer is accomplished with a recipe comprising gas SF_6 .

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17. The method of claim 1, wherein said depositing a second nitride layer is accomplished by CVD at a temperature between about 750 to 850°C by reacting dichlorosilane (SiCl_2H_2) with ammonia (NH_3).

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18. The method of claim 1, wherein said second nitride layer has a thickness between about 100 to 300 Å.

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19. The method of claim 1, wherein said second photoresist layer has a thickness between about 0.5 to 1.0 μm .

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20. The method of claim 1, wherein said etching through patterns in said second photoresist layer to form openings in said second nitride layer exposing portions of said first polysilicon layer is accomplished with a recipe comprising gases SF_6 , O_2 , Cl_2 and HBr .

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21. The method of claim 1, wherein said removing said second photoresist layer is accomplished by using oxygen plasma ashing.

22. The method of claim 1, wherein said performing thermal oxidation of said first polysilicon layer to form poly-oxide with a thickness between about 1000 to 1800 Å is accomplished by wet oxidation at a temperature between about 850 to 1000°C.

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23. The method of claim 1, wherein said etching said first polysilicon layer using said polyoxide as a hard mask is accomplished with a recipe comprising gases HBr, Cl₂ and O₂.

24. The method of claim 1, wherein said intergate oxide layer comprises oxynitride having a thickness between about 100 to 250 Å.

25. The method of claim 1, wherein said forming a second polysilicon layer is accomplished with silicon source SiH₄ using LPCVD at a temperature between about 500 to 650°C.

26. The method of claim 1, wherein said second polysilicon layer has a thickness between about 1000 to 3000 Å.

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27. The method of claim 1, wherein said third photoresist layer has a thickness between about 5000 to 10000 Å.

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28. The method of claim 1, wherein said etching through said patterning in third photoresist layer to complete the forming of said split-gate flash memory is accomplished with a recipe comprising HBr, Cl₂ and O₂.

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29. A method of forming a split-gate flash memory having a non-smiling trench isolation comprising the steps of:

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providing a semiconductor substrate;

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forming a trench;

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forming a first conformal lining on the inside walls of said trench;

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forming a second conformal lining over said first conformal lining on the inside walls of said trench;

forming conformal spacers;

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depositing isolation oxide inside said trench to form shallow trench isolation (STI);

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forming a floating gate;

21 forming an intergate oxide; and

forming a control gate to complete the forming of the split-
24 gate flash memory cell.

30. The method of claim 29, wherein said first conformal
lining comprises oxide having a thickness between about 200
3 to 550 Å.

31. The method of claim 29, wherein said second conformal
lining comprises nitride having a thickness between about
3 100 to 300 Å.

32. The method of claim 29, wherein said forming said
conformal spacers is accomplished by anisotropic etching of
3 second conformal lining

33. The method of claim 29, wherein said conformal spacers
have a thickness between about 100 to 300 Å.

34. A split-gate flash memory having a non-smiling trench
isolation comprising:

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a floating gate;

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a trench;

two conformal layers lining the inside walls of said trench;

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and

a control gate.

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35. The method of claim 34, wherein said first conformal
lining comprises oxide having a thickness between about 200
to 550 Å.

36. The method of claim 34, wherein said second conformal
lining comprises nitride having a thickness between about
100 to 300 Å.